

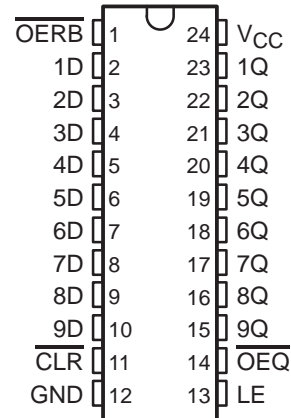
SN74ALS992

9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

SDAS028B – APRIL 1984 – REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- True Logic Outputs
- Designed With Nine Bits for Parity Applications
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

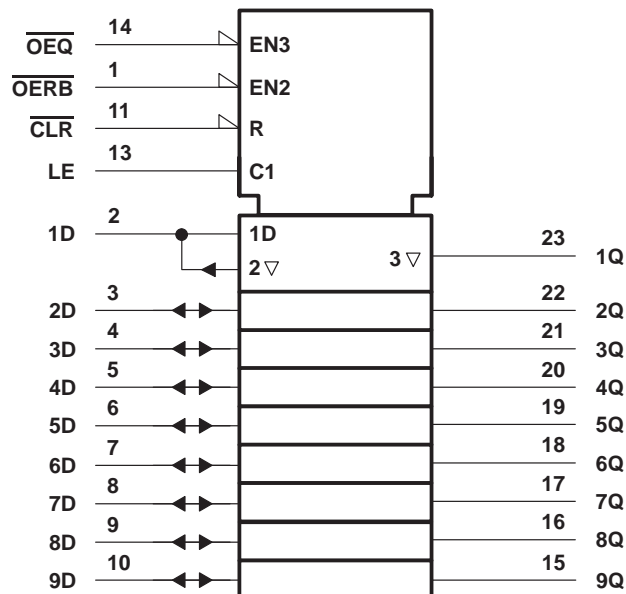
This 9-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. In addition, this device provides a 3-state buffer-type output and is easily implemented in parity applications.

The nine latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. The Q outputs are in the 3-state condition when the output-enable (\overline{OEQ}) input is high.

Read back is provided through the output-enable (\overline{OERB}) input. When \overline{OERB} is taken low, the data present at the output of the data latches is allowed to pass back onto the input data bus. When \overline{OERB} is taken high, the output of the data latches is isolated from the D inputs. \overline{OERB} does not affect the internal operation of the latches; however, precautions should be taken not to create a bus conflict.

The SN74ALS992 is characterized for operation from 0°C to 70°C.

logic symbol†



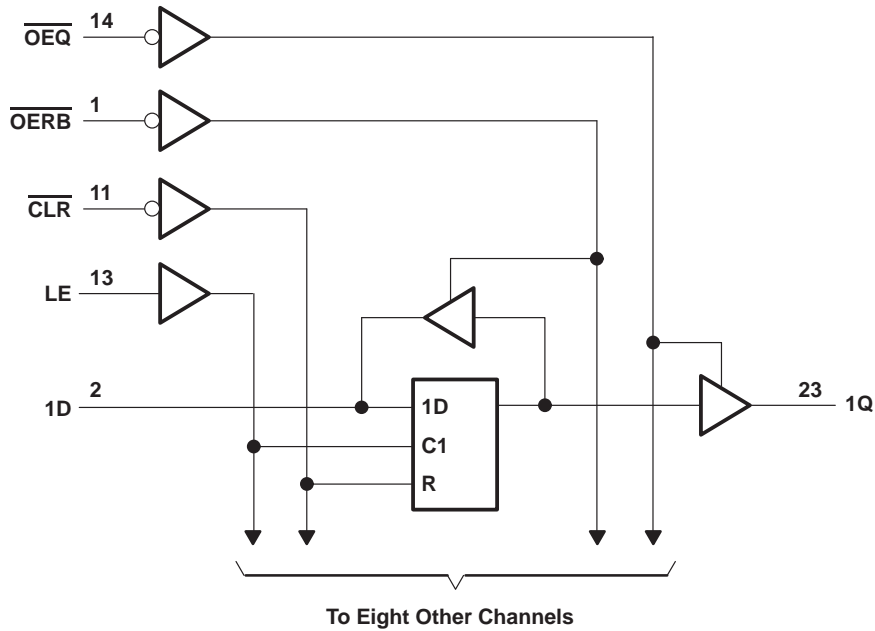
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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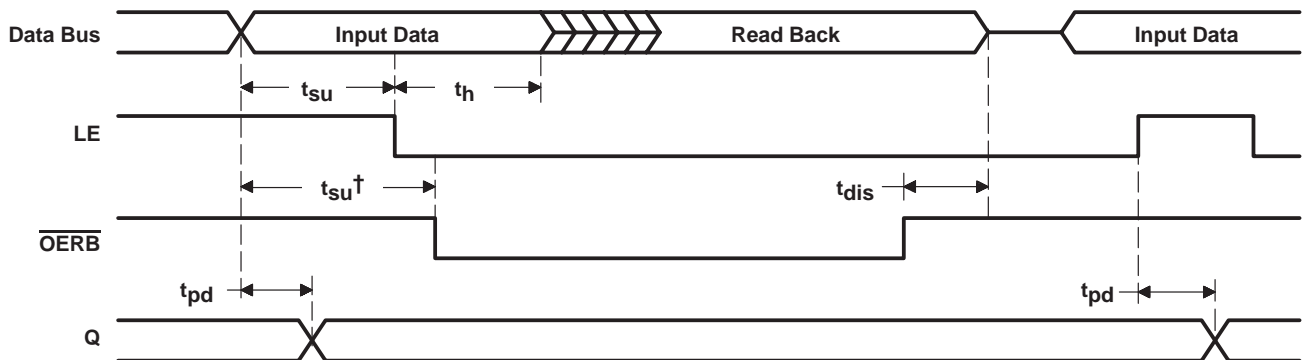
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logic diagram (positive logic)



timing diagram



$\overline{\text{CLR}} = \text{H}, \overline{\text{OEQ}} = \text{L}$

† This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I ($\overline{\text{OERB}}$, $\overline{\text{OEQ}}$, $\overline{\text{CLR}}$, and LE)	7 V
Voltage applied to D inputs and to disabled 3-state outputs	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q		-2.6	mA
		D		-0.4	
I_{OL}	Low-level output current	Q		24	mA
		D		8	
t_w	Pulse duration	LE high	10		ns
		CLR low	10		
t_{su}	Setup time	Data before LE↓	10		ns
		Data before \overline{OERB} ↓	10		
t_h	Hold time, data after LE↓	5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	All outputs	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			V
	Q	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -2.6\text{ mA}$	2.4	3.2		
V_{OL}	D	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V	
			$I_{OL} = 8\text{ mA}$	0.35	0.5		
	Q	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4		
			$I_{OL} = 24\text{ mA}$	0.35	0.5		
I_{OZH}	Q	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			20	μA
I_{OZL}	Q	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
I_I	D inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$			0.1	mA
	All others		$V_I = 7\text{ V}$			0.1	
I_{IH}	D inputs‡	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
	All others					20	
I_{IL}	D inputs‡	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.1	mA
	All others					-0.1	
$I_{OS}§$		$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-30		-112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, OERB high	Outputs high	30	50	mA	
			Outputs low	50	80		
			Outputs disabled	35	55		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 1)

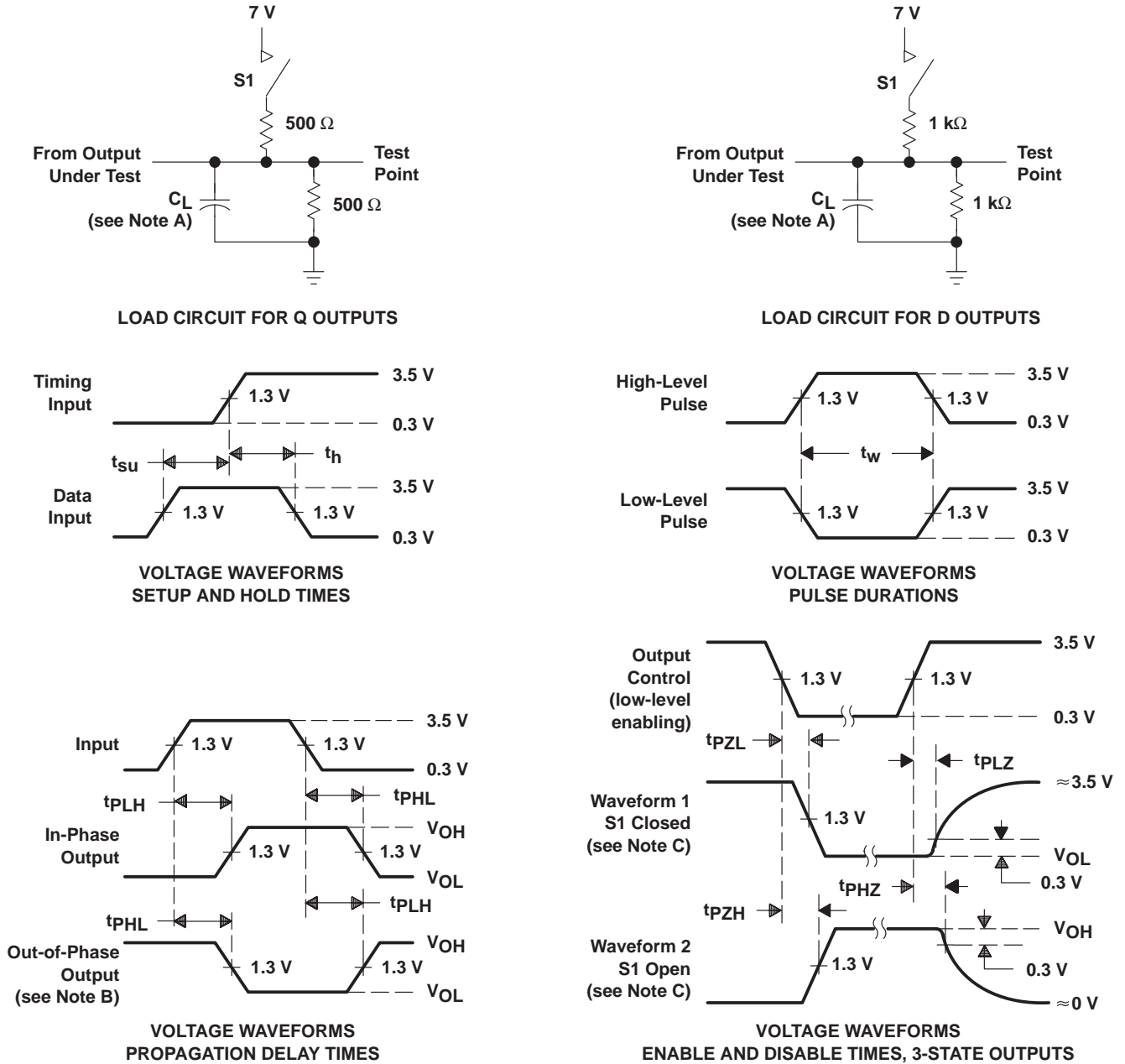
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = MIN to MAX†		UNIT
			MIN	MAX	
t _{PLH}	D	Q	3	14	ns
t _{PHL}			4	16	
t _{PLH}	LE	Q	6	20	ns
t _{PHL}			8	25	
t _{PHL}	$\overline{\text{CLR}}$	Q	6	20	ns
		D	8	26	
t _{en} ‡	$\overline{\text{OERB}}$	D	4	21	ns
t _{dis} §			2	14	
t _{en} ‡	$\overline{\text{OEQ}}$	Q	4	18	ns
t _{dis} §			1	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ t_{en} = t_{PZH} or t_{PZL}

§ t_{dis} = t_{PHZ} or t_{PLZ}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. When measuring propagation delay times of 3-state outputs, switch S1 is open.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS992DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS992DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS992DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS992DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS992DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS992NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS992NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS992DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



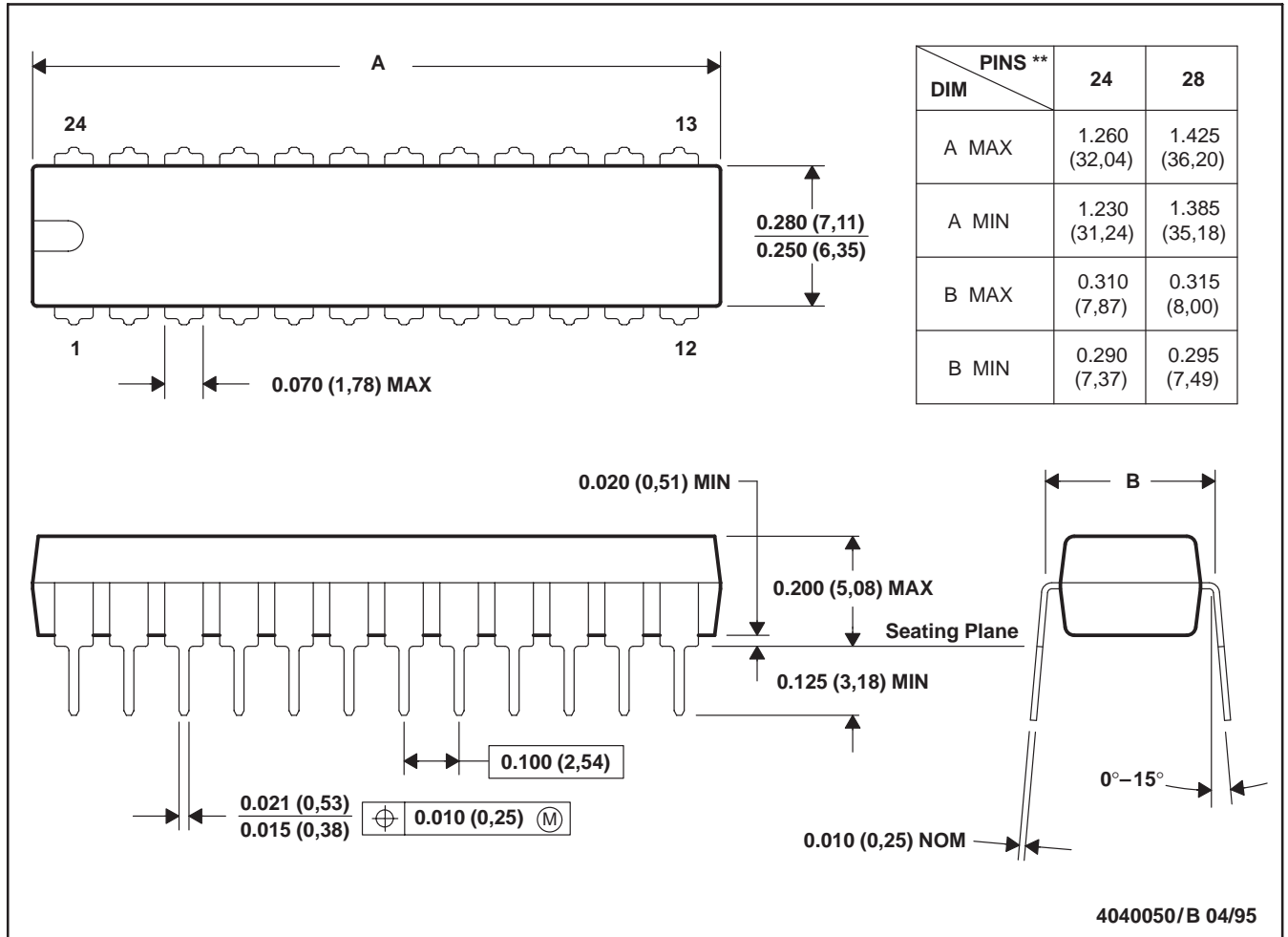
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS992DWR	SOIC	DW	24	2000	346.0	346.0	41.0

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

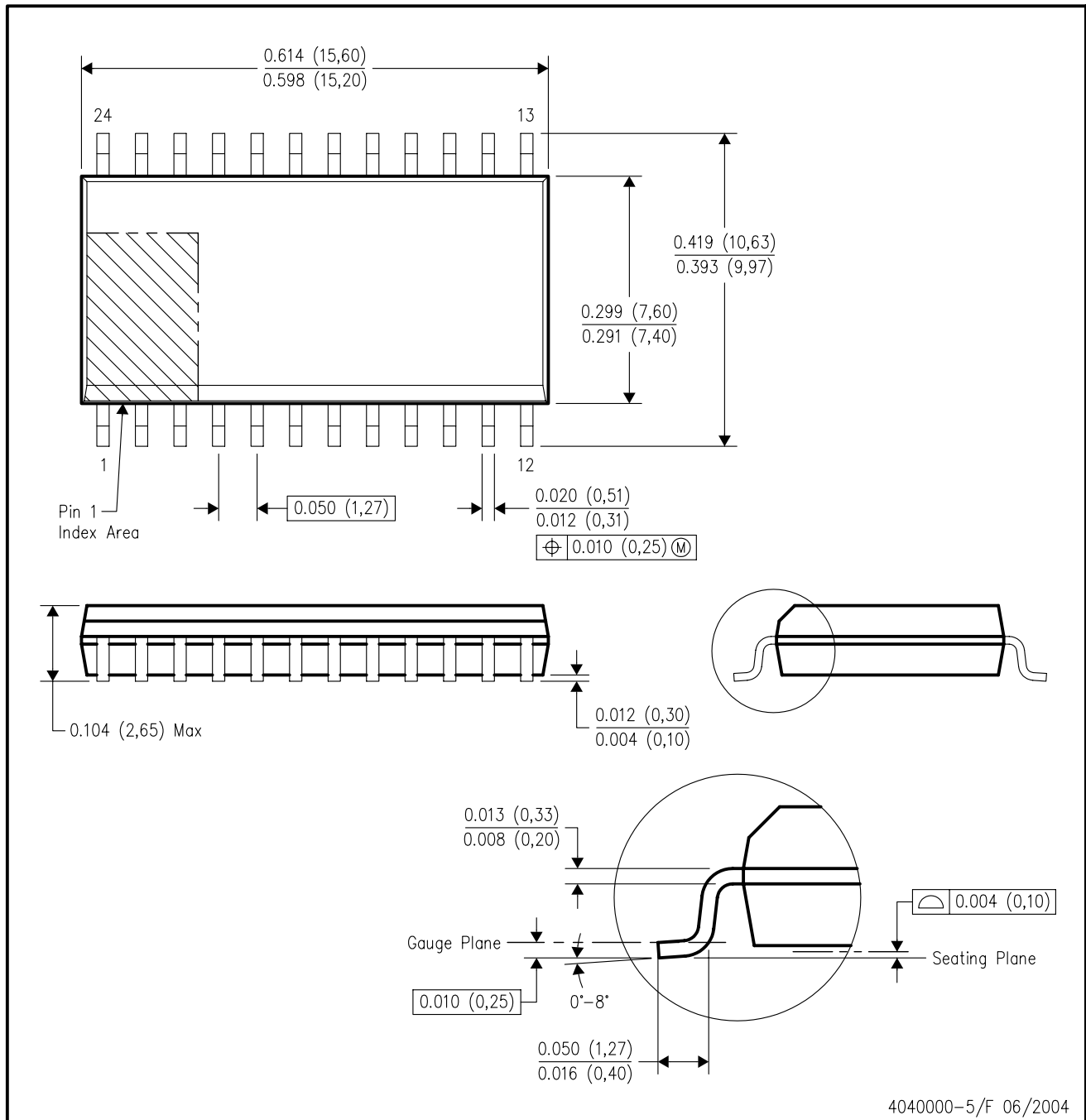
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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